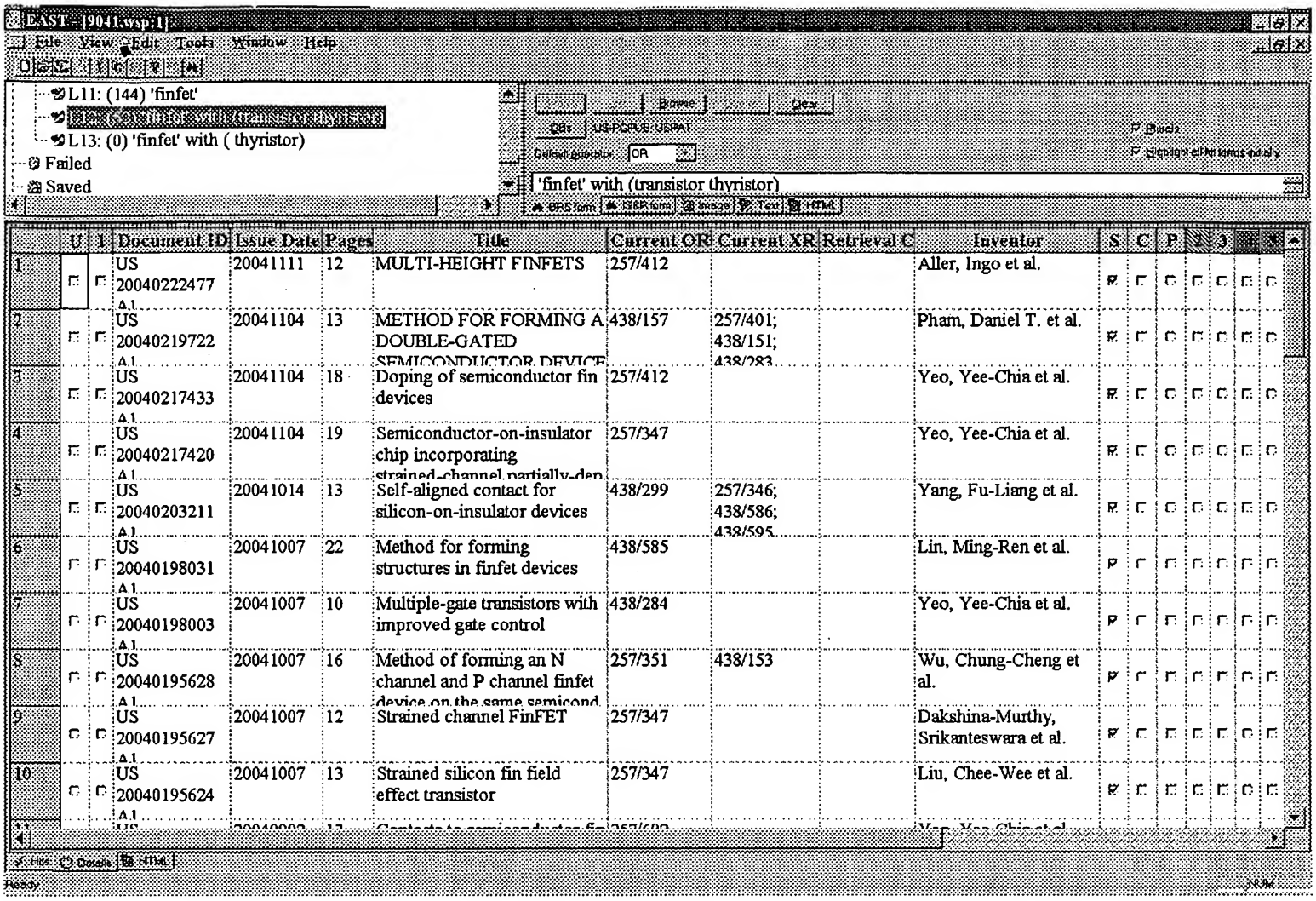
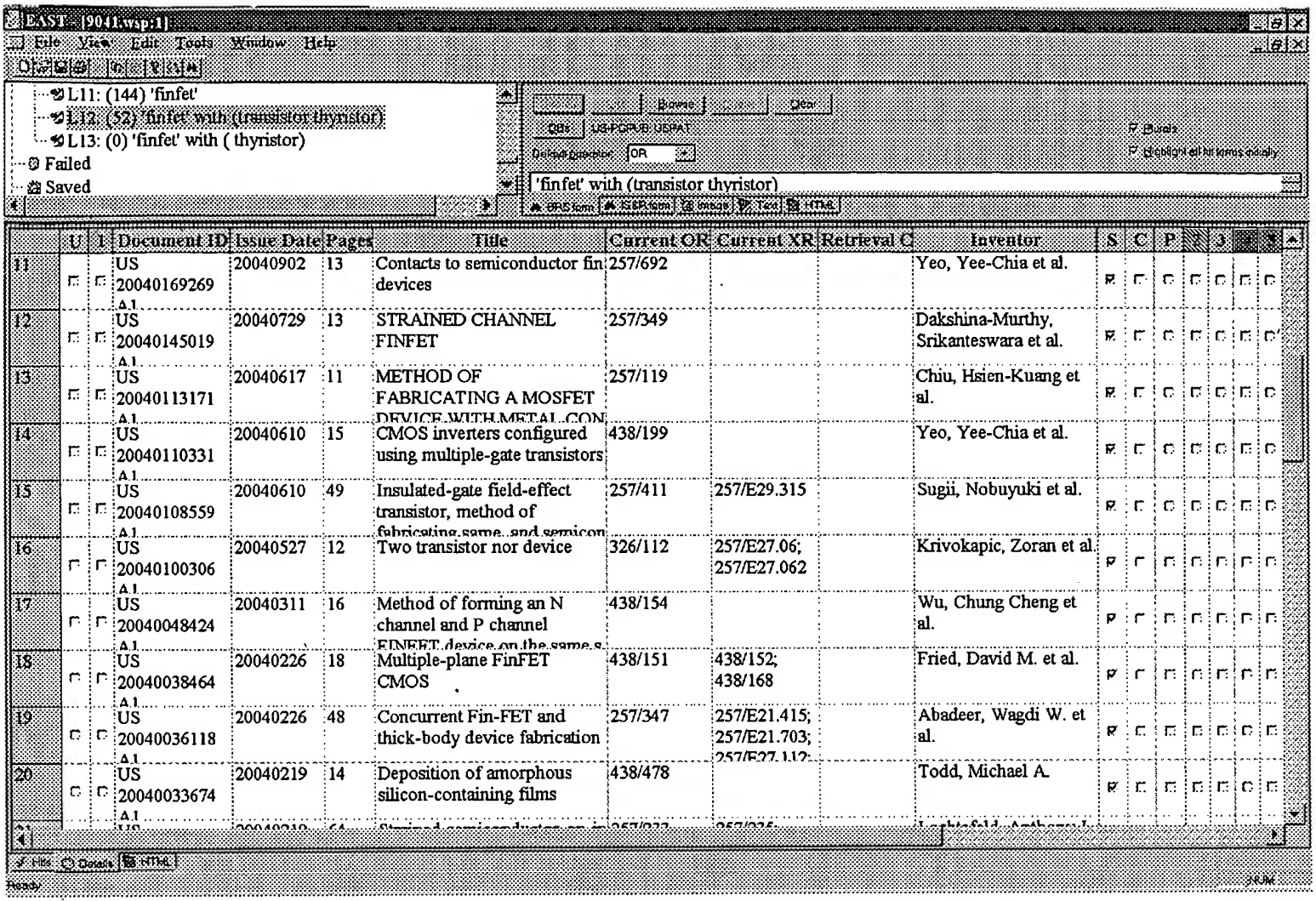
Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	10/629241	US-PGPUB; USPAT; EPO; JPO	OR	ON	2004/11/12 08:29
L2	0	10/629241	US-PGPUB; USPAT	OR	ON	2004/11/12 08:29
L3	0	10/629041	US-PGPUB; USPAT	OR	ON	2004/11/12 09:24
L4	5	"6492662"	US-PGPUB; USPAT	OR	ON	2004/11/12 09:27
L5	5	"6458632"	US-PGPUB; USPAT	OR	ON	2004/11/12 09:29
L6	10	"6448586"	US-PGPUB; USPAT	OR	ON	2004/11/12 09:32
L7	44	"6229161"	US-PGPUB; USPAT	OR	ON	2004/11/12 10:22
L8	24	thyristor with transistor.ti.	US-PGPUB; USPAT	OR	ON	2004/11/12 10:23
L9	951	thyristor with transistor.clm.	US-PGPUB; USPAT	OR	ON	2004/11/12 10:24
L10	64	(thyristor with transistor) with (method process).clm.	US-PGPUB; USPAT	OR	ON	2004/11/12 10:26
L11	144	'finfet'	US-PGPUB; USPAT	OR	ON	2004/11/12 10:48
L12	52	'finfet' with (transistor thyristor)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:52
L13	0	'finfet' with (thyristor)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:32
L14	40	'finfet'.TI.	US-PGPUB; USPAT	OR	ON	2004/11/12 10:49
L15	0	14 AND ('finfet' WITH THYRISTOR)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:50
L16	0	14 AND (TRANSISTOR WITH THYRISTOR)	US-PGPUB; USPAT	OR	ON	2004/11/12 10:50
L17	0	14 AND (FINFET WITH (TRANSISTOR WITH THYRISTOR))	US-PGPUB; USPAT	OR	ON	2004/11/12 10:51
L18	0	12 AND THYRISTOR	US-PGPUB; USPAT	OR	ON	2004/11/12 10:52

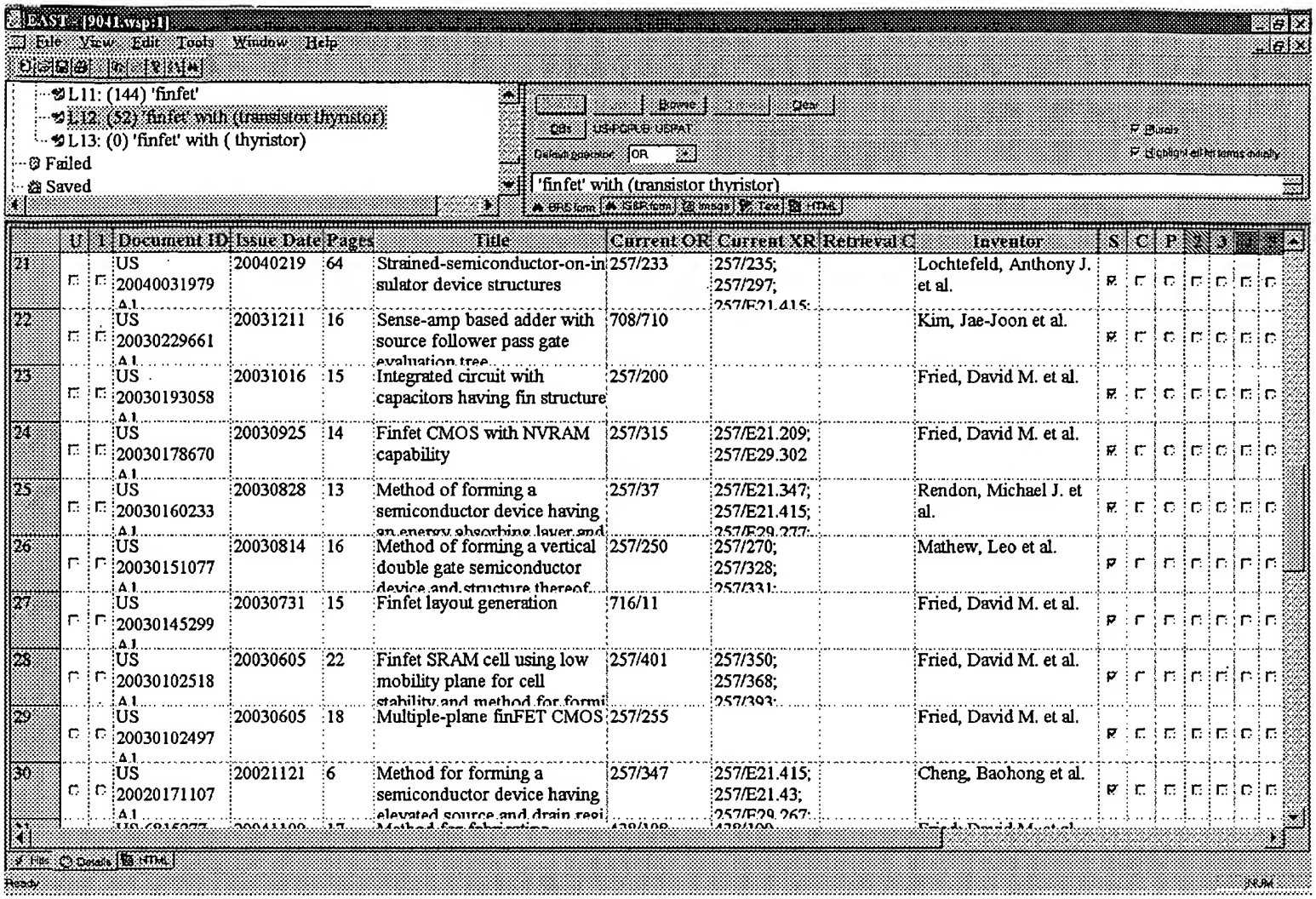
L19	0	'finfet' with thyristor	US-PGPU B; USPAT	OR	ON	2004/11/12 10:52
L20	7	11 AND thyristor	US-PGPU B; USPAT	OR	ON	2004/11/12 10:52



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	2	3
1			US 20040222477 A1	20041111	12	MULTI-HEIGHT FINFETS	257/412			Aller, Ingo et al.					
2			US 20040219722 A1	20041104	13	METHOD FOR FORMING A DOUBLE-GATED SEMICONDUCTOR DEVICE	438/157	257/401; 438/151; 438/283		Pham, Daniel T. et al.					
3			US 20040217433 A1	20041104	18	Doping of semiconductor fin devices	257/412			Yeo, Yee-Chia et al.					
4			US 20040217420 A1	20041104	19	Semiconductor-on-insulator chip incorporating strained-channel partially-dep	257/347			Yeo, Yee-Chia et al.					
5			US 20040203211 A1	20041014	13	Self-aligned contact for silicon-on-insulator devices	438/299	257/346; 438/586; 438/595		Yang, Fu-Liang et al.					
6			US 20040198031 A1	20041007	22	Method for forming structures in finfet devices	438/585			Lin, Ming-Ren et al.					
7			US 20040198003 A1	20041007	10	Multiple-gate transistors with improved gate control	438/284			Yeo, Yee-Chia et al.					
8			US 20040195628 A1	20041007	16	Method of forming an N channel and P channel finfet device on the same semicond	257/351	438/153		Wu, Chung-Cheng et al.					
9			US 20040195627 A1	20041007	12	Strained channel FinFET	257/347			Dakshina-Murthy, Srikanteswara et al.					
10			US 20040195624 A1	20041007	13	Strained silicon fin field effect transistor	257/347			Liu, Chee-Wee et al.					
11			US												



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P	2	3	4	5
11			US 20040169269 A1	20040902	13	Contacts to semiconductor fin devices	257/692			Yeo, Yee-Chia et al.							
12			US 20040145019 A1	20040729	13	STRAINED CHANNEL FINFET	257/349			Dakshina-Murthy, Srikanteswara et al.							
13			US 20040113171 A1	20040617	11	METHOD OF FABRICATING A MOSFET DEVICE WITH METAL CON	257/119			Chiu, Hsien-Kuang et al.							
14			US 20040110331 A1	20040610	15	CMOS inverters configured using multiple-gate transistors	438/199			Yeo, Yee-Chia et al.							
15			US 20040108559 A1	20040610	49	Insulated-gate field-effect transistor, method of fabricating same, and semicon	257/411	257/E29.315		Sugii, Nobuyuki et al.							
16			US 20040100306 A1	20040527	12	Two transistor nor device	326/112	257/E27.06; 257/E27.062		Krivokapic, Zoran et al.							
17			US 20040048424 A1	20040311	16	Method of forming an N channel and P channel FINFET device on the same s	438/154			Wu, Chung Cheng et al.							
18			US 20040038464 A1	20040226	18	Multiple-plane FinFET CMOS	438/151	438/152; 438/168		Fried, David M. et al.							
19			US 20040036118 A1	20040226	48	Concurrent Fin-FET and thick-body device fabrication	257/347	257/E21.415; 257/E21.703; 257/E27.112		Abadeer, Wagdi W. et al.							
20			US 20040033674 A1	20040219	14	Deposition of amorphous silicon-containing films	438/478			Todd, Michael A.							


EAST - [9041.wsp:1]
File View Edit Tools Window Help
L11: (144) 'finfet'
L12: (52) 'finfet' with (transistor thyristor)
L13: (0) 'finfet' with (thyristor)
Failed
Saved
Browse
Clear
DBs
USPGPUB USPAT
Default operator
OR
Bools
Highlight all hit terms easily
'finfet' with (transistor thyristor)
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Issue Date
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Current OR
Current XR
Retrieval C
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21 US 20040031979 A1 20040219 64 Strained-semiconductor-on-insulator device structures 257/233 257/235; 257/297; Lochtefeld, Anthony J. et al.
22 US 20030229661 A1 20031211 16 Sense-amp based adder with source follower pass gate evaluation tree 708/710 Kim, Jae-Joon et al.
23 US 20030193058 A1 20031016 15 Integrated circuit with capacitors having fin structure 257/200 Fried, David M. et al.
24 US 20030178670 A1 20030925 14 Finfet CMOS with NVRAM capability 257/315 257/E21.209; 257/E29.302 Fried, David M. et al.
25 US 20030160233 A1 20030828 13 Method of forming a semiconductor device having an energy absorbing layer and 257/37 257/E21.347; 257/E21.415; Rendon, Michael J. et al.
26 US 20030151077 A1 20030814 16 Method of forming a vertical double gate semiconductor device and structure thereof 257/250 257/270; 257/328; Mathew, Leo et al.
27 US 20030145299 A1 20030731 15 Finfet layout generation 716/11 Fried, David M. et al.
28 US 20030102518 A1 20030605 22 Finfet SRAM cell using low mobility plane for cell stability and method for formi 257/401 257/350; 257/368; Fried, David M. et al.
29 US 20030102497 A1 20030605 18 Multiple-plane finFET CMOS 257/255 Fried, David M. et al.
30 US 20020171107 A1 20021121 6 Method for forming a semiconductor device having elevated source and drain regi 257/347 257/E21.415; 257/E21.43; Cheng, Baohong et al.
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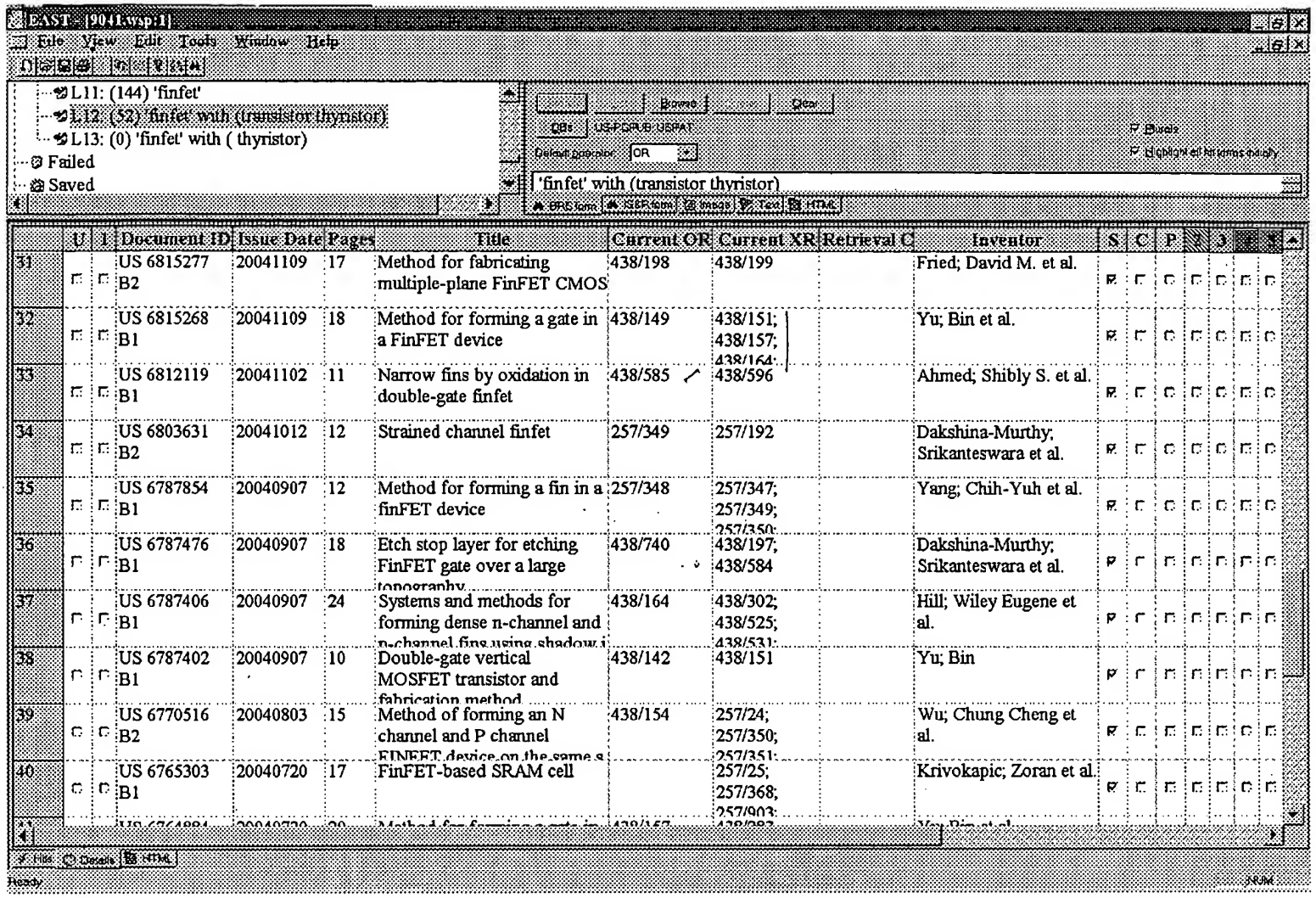
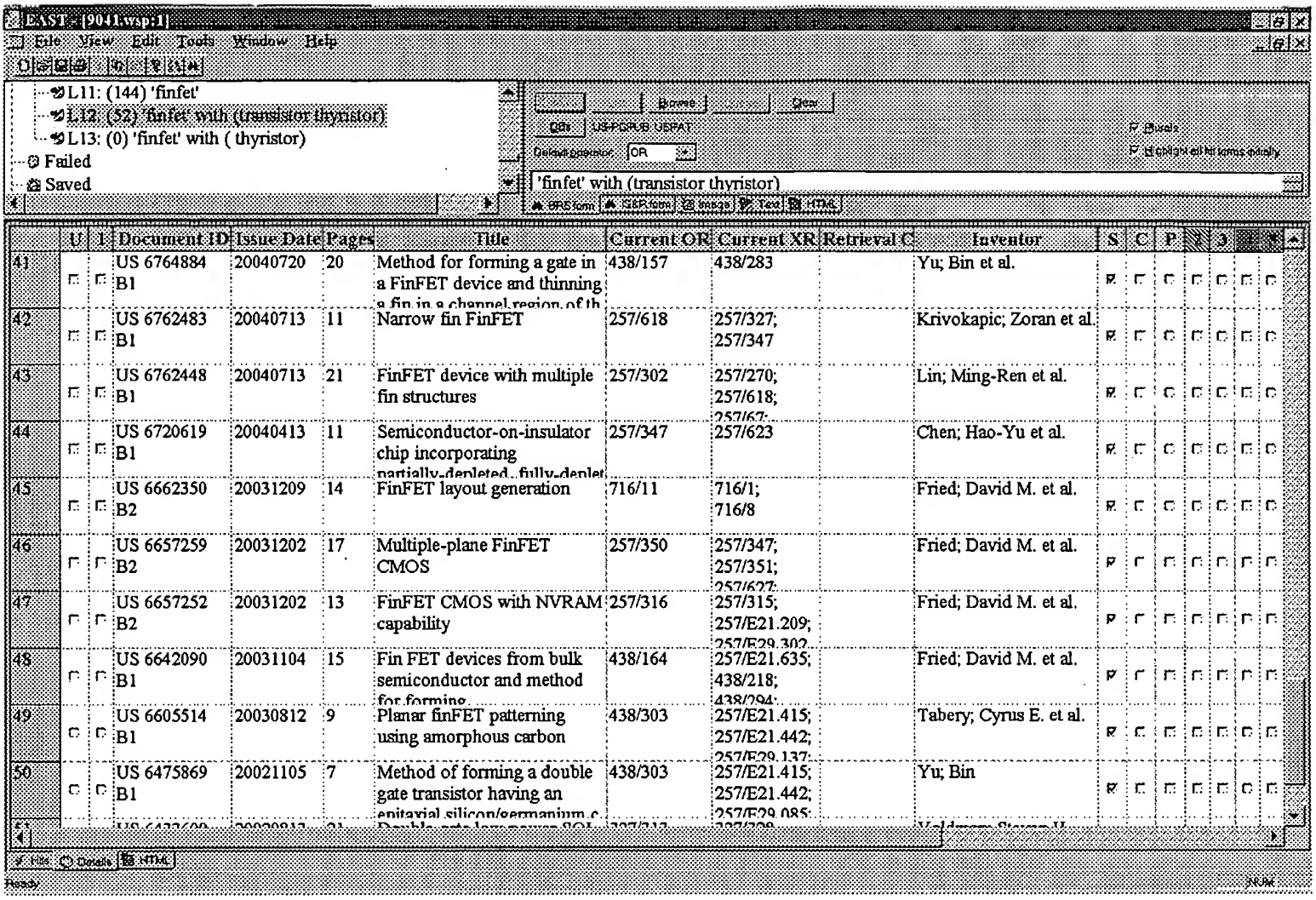


	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P
31	☐	☐	US 6815277 B2	20041109	17	Method for fabricating multiple-plane FinFET CMOS	438/198	438/199		Fried; David M. et al.	☑	☐	☐
32	☐	☐	US 6815268 B1	20041109	18	Method for forming a gate in a FinFET device	438/149	438/151; 438/157; 438/164;		Yu; Bin et al.	☑	☐	☐
33	☐	☐	US 6812119 B1	20041102	11	Narrow fins by oxidation in double-gate finfet	438/585	438/596		Ahmed; Shibly S. et al.	☑	☐	☐
34	☐	☐	US 6803631 B2	20041012	12	Strained channel finfet	257/349	257/192		Dakshina-Murthy; Srikanteswara et al.	☑	☐	☐
35	☐	☐	US 6787854 B1	20040907	12	Method for forming a fin in a finFET device	257/348	257/347; 257/349; 257/350;		Yang; Chih-Yuh et al.	☑	☐	☐
36	☐	☐	US 6787476 B1	20040907	18	Etch stop layer for etching FinFET gate over a large topography	438/740	438/197; 438/584		Dakshina-Murthy; Srikanteswara et al.	☑	☐	☐
37	☐	☐	US 6787406 B1	20040907	24	Systems and methods for forming dense n-channel and p-channel fins using shadow i	438/164	438/302; 438/525; 438/531;		Hill; Wiley Eugene et al.	☑	☐	☐
38	☐	☐	US 6787402 B1	20040907	10	Double-gate vertical MOSFET transistor and fabrication method	438/142	438/151		Yu; Bin	☑	☐	☐
39	☐	☐	US 6770516 B2	20040803	15	Method of forming an N channel and P channel FINFET device on the same s	438/154	257/24; 257/350; 257/351;		Wu; Chung Cheng et al.	☑	☐	☐
40	☐	☐	US 6765303 B1	20040720	17	FinFET-based SRAM cell		257/25; 257/368; 257/903;		Krivokapic; Zoran et al.	☑	☐	☐



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XR	Retrieval C	Inventor	S	C	P				
41			US 6764884 B1	20040720	20	Method for forming a gate in a FinFET device and thinning a fin in a channel region of th	438/157	438/283		Yu; Bin et al.							
42			US 6762483 B1	20040713	11	Narrow fin FinFET	257/618	257/327; 257/347		Krivokapic; Zoran et al.							
43			US 6762448 B1	20040713	21	FinFET device with multiple fin structures	257/302	257/270; 257/618; 257/67;		Lin; Ming-Ren et al.							
44			US 6720619 B1	20040413	11	Semiconductor-on-insulator chip incorporating partially-depleted, fully-deplet	257/347	257/623		Chen; Hao-Yu et al.							
45			US 6662350 B2	20031209	14	FinFET layout generation	716/11	716/1; 716/8		Fried; David M. et al.							
46			US 6657259 B2	20031202	17	Multiple-plane FinFET CMOS	257/350	257/347; 257/351; 257/627;		Fried; David M. et al.							
47			US 6657252 B2	20031202	13	FinFET CMOS with NVRAM capability	257/316	257/315; 257/E21.209; 257/E29.302		Fried; David M. et al.							
48			US 6642090 B1	20031104	15	Fin FET devices from bulk semiconductor and method for forming	438/164	257/E21.635; 438/218; 438/294;		Fried; David M. et al.							
49			US 6605514 B1	20030812	9	Planar finFET patterning using amorphous carbon	438/303	257/E21.415; 257/E21.442; 257/E29.137;		Tabery; Cyrus E. et al.							
50			US 6475869 B1	20021105	7	Method of forming a double gate transistor having an epitaxial silicon/germanium c	438/303	257/E21.415; 257/E21.442; 257/E29.085;		Yu; Bin							
51			US 6437600	20020813	21	Double-gate low-power SOI	327/212	327/208		Voldman; Steven H.							